
# PXI–Based Semiconductor Test Systems

## Advanced Test Capabilities and Features

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## Overview

The ongoing challenge for today's semiconductor test engineers is to identify and create new test solutions that can offer significantly lower test costs as well as address the need for configurable, open-architecture, flexible test solutions that can provide comparable features to proprietary ATE platforms. In particular, for test requirements with low to moderate volumes – i.e. pilot production, verification, and focused production test applications, the need for flexible and cost effective ATE solutions is particularly acute. For these applications, test engineers historically have relied upon legacy test systems which have a low acquisition cost but high operating costs or in-house designed, rack and stack solutions. However, semiconductor test system solutions based on the PXI platform have made significant advancements in functionality and performance over the past 3 or 4 years, offering test engineers a viable alternative for both current and future test needs.

For digital and SoC test applications, today's PXI test systems offer moderate to high digital channel count capability with parametric measurement unit (PMU) per pin functionality. However, existing PXI digital subsystems have been largely limited to verifying DC and functional test characteristics of a device due to their limited timing engine capabilities. To fully meet the test requirements found in "big ATE", a PXI based test system (and its digital subsystem) must also be capable of testing a device's AC characteristics, e.g. setup and hold times – a capability that has not been easily achieved by the current generation of PXI instruments. The latest generation of PXI systems and instrumentation offers many of the features found in proprietary ATE systems, including an advanced timing engine and software tools for importing test vectors and developing test programs.

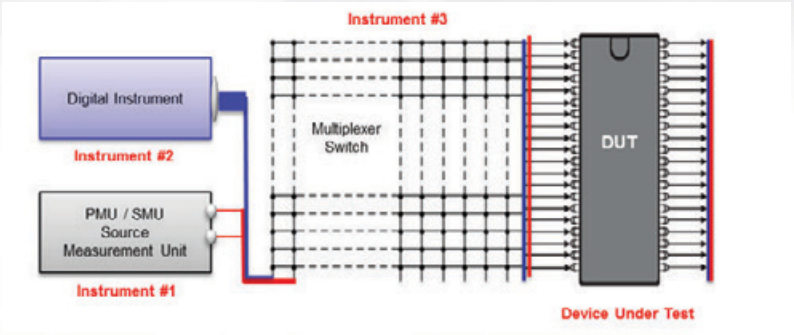


Figure 1 – System Configuration with PMU, Digital Instrument and Switching Matrix

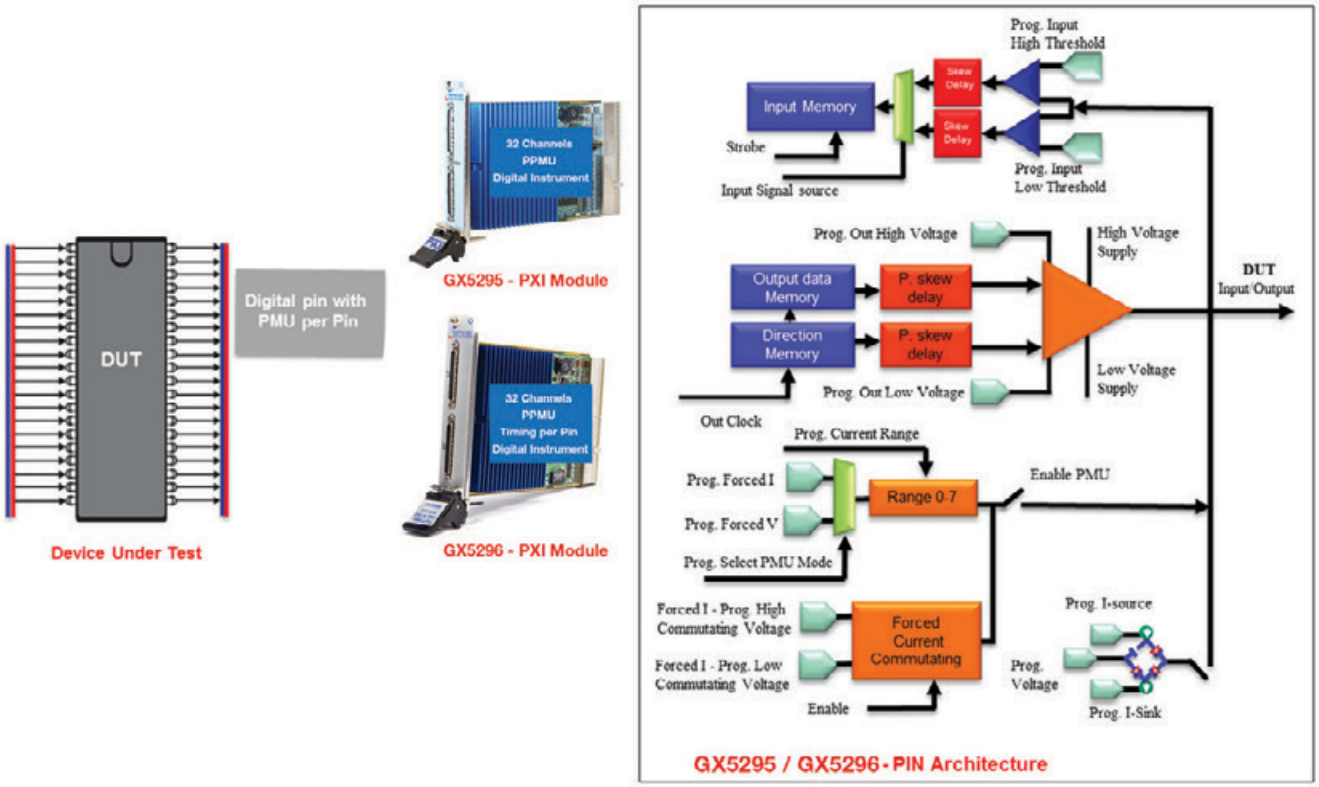


Figure 2 – 3U PXI, 32 Channel Digital I/O with per pin PMU Architecture

## Semiconductor Test Requirements

The basic test needs for digital and mixed-signal devices include DC / AC parametric and functional tests. For the DC tests, all of a device's pins must be characterized which requires a PMU (parametric measurement unit). A PMU, which can source voltage / measure current or source current / measure voltage, must be able to access all of the device's pins which require some type of switching / multiplexer if a single PMU is used. Once DC characterization is completed functional / AC parametric testing of the device can be performed. In this case, a digital instrument with sufficiently deep memory, per channel programmability (voltage, loads, and direction), programmable edge placement and real-time compare provides the key features for testing AC parametrics and functionality. A basic setup that addresses these capabilities is shown in Figure 1.

The configuration shown in Figure 1 is not practical for even moderate pin count ATE systems. Today's PXI test systems incorporate a PMU per pin or channel architecture, offering high channel count configurations and superior test performance (both for speed and measurement accuracy). Figure 2 details the architecture of a digital instrument that includes a PMU per pin configuration. PXI Test Systems such as Marvin Test Solutions' TS-900 series which features up to 512 digital I/O channels with a per pin PMU architecture offers users a high channel count digital and mixed-signal test system in a small, compact, single PXI chassis. (Figure 3)

## Performing DC Parametric Tests

As noted previously, a PMU can be used in one of two modes to perform DC characterization tests on the input and output pins of digital devices:

- Force voltage and measure current. With this method the PMU applies a constant voltage and using its on-board measurement capability it measures the current being drawn by the device/pin being tested. The voltage being supplied by the PMU can also be measured.
- Force current and measure voltage. With this method the parametric measurement unit either forces a constant current across a device or sinks a constant current from a device pin and then measures the resultant voltage. The PMU sink/source current also can be measured.

By combining a PMU per channel with digital test capabilities in one instrument, performing a range of DC tests on digital and mixed signal devices is significantly simplified. Common DC tests performed on digital devices include input voltage levels (VIH/VIL), output voltage levels (VOL/VOH), input leakage and output short circuit current tests.

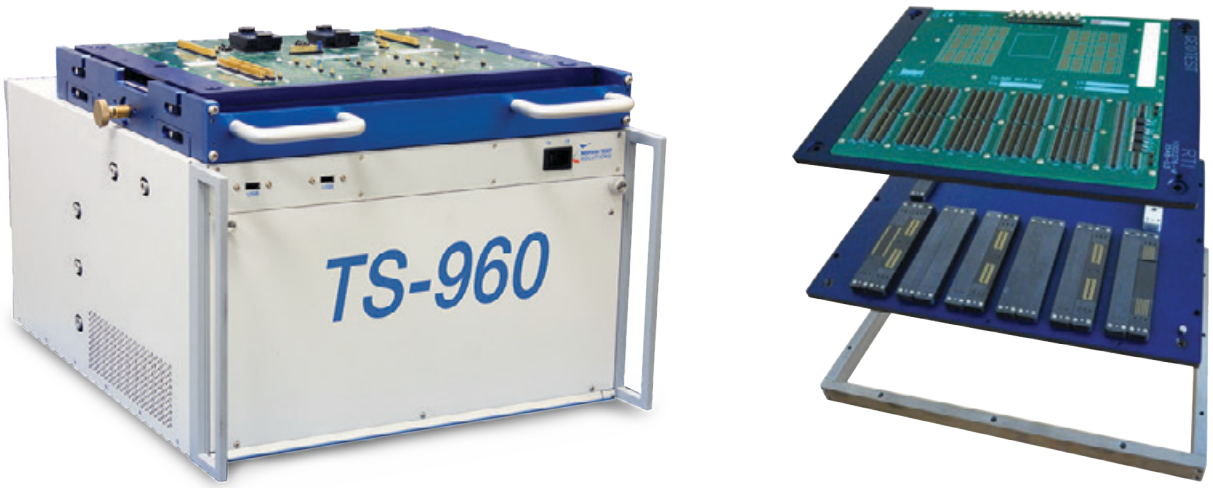


Figure 3 – TS-960 PXI Semiconductor Test System with pogo pin receiver and selftest board

## Example: Performing Input Leakage Test (IIL, IIH) and V-I Tests

Testing a device's inputs includes leakage current testing as well as characterizing the protection diodes present on each input of the DUT. These tests are performed by applying a constant voltage, in steps over a specified test voltage range, to the DUT input pin and measuring the input current at each step (Figure 4). As leakage currents are often in the uA range, the PMU should be set to its more sensitive current ranges to achieve more accurate measurements.

To perform an Input Leakage Test the DUT is powered up and the PMU pin is set to Force Voltage/ Measure Current Mode. At each input voltage setting the PMU measures the current being drawn by the input and then verifies the value against the DUT specification. The actual test voltage that the PMU is sourcing can be measured as well.

The testing technique can also be used for VIL and VIH testing.

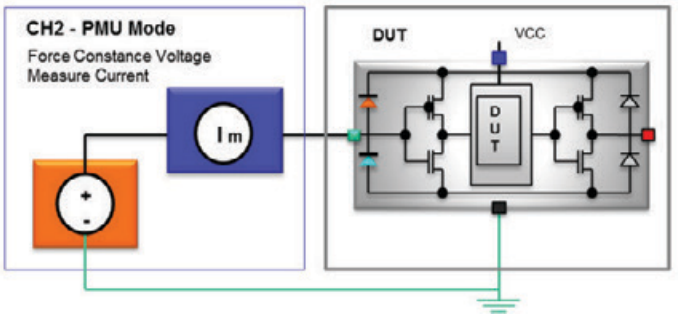


Figure 4: Input Leakage test using the digital instrument's PMU capability

For measuring / characterizing the input protection diodes which are connected to the device's ground and VCC pins, the PMU is configured for force voltage / measure current with the voltage stepped in small increments in order to produce V-I curve for each diode. Figure 5 shows the protection diode V-I curves for a TTL digital device. Note that the device begins to conduct at a junction voltage of about 0.7 volts.

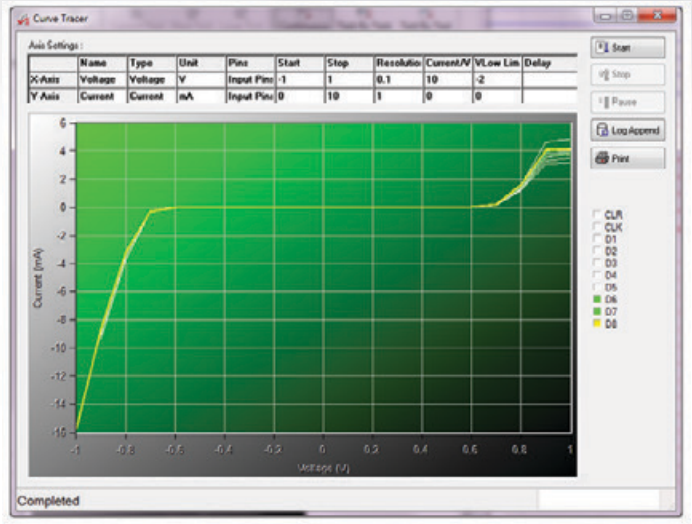


Figure 5 – V-I Curve Characterizing a DUT's Input Protection Diodes

The development of these tests can be greatly simplified by employing software tools and libraries. Tools such as Marvin Test Solutions' ICEasy provide the user with the ability to automate the creation of I-V curves, 2-D Shmoo plots as well as automatically generating the parametric DC device tests.

## AC Parametric Test Capabilities

To adequately address the capabilities and functionality found in proprietary big iron ATE digital instrumentation, today's PXI –based digital subsystem must have flexible and dynamic timing per pin or channel capability. Unlike existing 3U PXI digital subsystems which employ a "singular" timing system which means all I/O channels are clocked with the same clock edge, a dynamic timing per pin system provides the flexibility to position data independently and dynamically on a per channel basis. Additionally, data formatting (e.g. non return to zero or return to zero, etc.) offers added flexibility when emulating complex bus timing or if testing for pulse width sensitivity. With these dynamic timing features and data formatting, a PXI-based test system can offer the test capabilities that are comparable to "big iron" ATE systems.

Dynamic timing implies the ability to move edges anywhere within a test step with adequate resolution. The challenge for a singular timing system is that edge placement will be limited to a rising or falling edge of the vector clock rate and edge placement will be fixed for a complete vector burst. For example, if the vector clock rate is 100MHz, edge placement will be limited 5ns resolution with slower clock rates resulting in proportionally less resolution. To adequately characterize and test digital devices with toggle rates of 100 MHz or more, a test system must be able to move incrementally and dynamically, data / clock edges with 1ns resolution or better. A typical application is characterization of a device's setup and hold times, which requires incremental movement of data, relative to a clock (Figure 6).

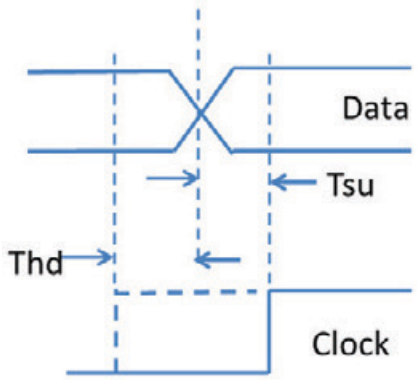


Figure 6 – Setup and Hold Test

To perform this test, data (or clock) is moved relative to the clock (or data) in small increments allowing full AC characterization of the device. Using the digital subsystem's multiple time set feature, it is possible to assign a different value for sequence or test step, allowing the clock edge to be incremented through the device's specified setup and hold timing range.

The solution to providing adequate timing resolution without resorting to 1 GHz or greater timing clock rates, is to employ a dynamic timing interpolator, which provides the flexibility to position drive / sense test vectors anywhere within a test step with 1 ns or better resolution – not just on the vector clock's edge boundary. This flexibility allows users to precisely create vector timing without resulting to work- arounds such as over-sampling, a technique which employs the use of multiple vectors in order to achieve even moderate edge placement resolution. In addition, the ability to "dynamically" program a pin's timing vastly simplifies the creation / execution of timing Shmoo plots, validation /characterization of a device's AC parametrics, and offers easier conversion of WGL, STIL and VCD test vectors. Performing these tests with an instrument that supports only "static" timing per pin requires much longer test times and in some cases, the instrument's capabilities may just not be adequate for the application.

The table below highlights the capabilities of the advanced PXI digital I/O digital subsystem with a timing per pin architecture, compared to a singular timing architecture.

| Feature | Timing Per Pin Architecture (125 MHz T0 Clock) | Singular Timing Engine (200 MHz Max Vector Rate) |
|---|---|---|
| Edge placement | 1 ns – dynamic, programmable for each sequence step. | 5ns –fixed, static; conversion of test vectors can require timing coercion to adapt vector test files. |
| Requires multiple vectors to achieve edge resolution (over sampling) | No | Yes |
| Data formatting & programmable assert / de-assert edges | Yes, 6 formats; NR, RT0, RT1, RZ, RTC, SBC | No |
| Multiple time sets: emulate various bus timing cycles | Yes, up to 64, selectable per sequence step | No ( requires linearization of test sequence vectors and oversampling) |

By combining the features of a timing per pin architecture with software tools, the dynamic performance of digital and mixed signal devices can be readily characterized. For example by employing a two dimensional Shmoo plot, a device's performance can be characterized based upon power supply variations or other parameters. Returning to the setup and hold example, figure 7 details Shmoo plots for these two parameters versus power supply variations. In each case, test vectors were applied to the device under test (DUT) over a range of timing and power supply conditions with pass / fail results being displayed for each specific operating condition.

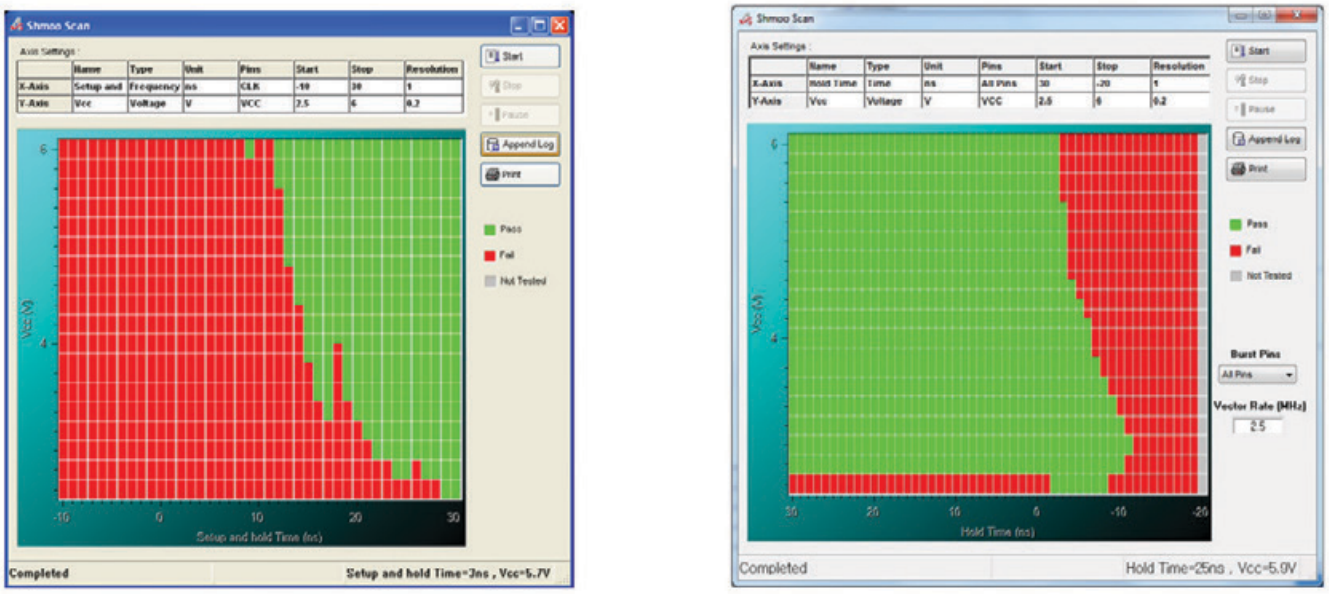


Figure 7 – Setup and Hold Shmoo Plots

## Summary

The next generation of PXI digital instrumentation offers the capabilities and test features normally only found in proprietary ATE semiconductor systems. With the advent of these new, advanced digital subsystems, PXI–based semiconductor test solutions such as the TS-900 can now offer a broader range of test capabilities and features for digital, mixed-signal and RF test applications. Offering comparable features and performance to proprietary or "big iron" ATE, today's PXI systems offer compelling test solutions for verification, focused production, and failure analysis applications. With a wide offering of software tools, an intuitive software development / test executive environment (ATEasy), and the open architecture of PXI, PXI platforms like the TS-900 offer a cost effective, performance ATE solution.

To learn more:
TS-960 Semiconductor Test System
GX5296 PXI Digital Instrument